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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/542,250	07/15/2005	Yasuyuki Teranishi	SON-2901	1363
23353 DADED EISHI	7590 08/01/2007 MAN & GRAUER PLLC		EXAMINER	
LION BUILDING 1233 20TH STREET N.W., SUITE 501 WASHINGTON, DC 20036			HAILEMARIAM, EMMANUEL	
			ART UNIT	PAPER NUMBER
WASHINGTO	11, 20 20000		2629	
	,		MAIL DATE	DELIVERY MODE
			08/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)				
Office Action Summan	10/542,250	TERANISHI ET AL.				
Office Action Summary	Examiner	Art Unit				
	Emmanuel Hailemariam	2629				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the	correspondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DATE - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  If NO period for reply is specified above, the maximum statutory period was reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATIO 36(a). In no event, however, may a reply be ting ATE OF THIS COMMUNICATION  ATE OF THIS COMUNICATION  ATE OF THIS COMMUNICATION  ATE OF THIS COMMUNICATION	N. mely filed the mailing date of this communication. ED (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 06/14	<u>//07</u> .					
2a) This action is <b>FINAL</b> . 2b) ⊠ This	This action is <b>FINAL</b> . 2b)⊠ This action is non-final.					
• • •	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under E	x parte Quayle, 1935 C.D. 11, 4	53 O.G. 213.				
Disposition of Claims						
4)⊠ Claim(s) <u>1-3</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdraw	vn from consideration.					
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-3</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or	election requirement.					
Application Papers						
9) The specification is objected to by the Examine	r.					
10)⊠ The drawing(s) filed on <u>07/15/05</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Ex	aminer. Note the attached Office	e Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for foreign a)⊠ All b)□ Some * c)□ None of:	priority under 35 U.S.C. § 119(a	)-(d) or (f).				
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
<ol><li>Copies of the certified copies of the prior</li></ol>	ity documents have been receiv	ed in this National Stage				
application from the International Bureau						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) Notice of References Cited (PTO-892)	4) Interview Summary					
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08)	Paper No(s)/Mail D 5) Notice of Informal f					
Paper No(s)/Mail Date <u>07/15/2005</u> .	6) Other:					

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of group I, which includes claims 1-3 in the

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reply filed on 06-14-2007 is acknowledged. The traversal is on the ground(s) that there

is not as serious burden on the examiner. This is not found persuasive because

contrary to applicant remarks, a search for and application of prior art to the various

species are in fact a burden on the office. Therefore the requirement is still deemed

proper and is therefore made FINAL.

**Drawings** 

Figures 1-3 should be designated by a legend such as -- Prior Art-- because only

See MPEP § 608.02(g). Corrected drawings in that which is old is illustrated.

compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid

abandonment of the application. The replacement sheet(s) should be labeled

"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office

action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) (Fig. 1-3) in view of Nakajima (EP 1 014334 A2).

AS to claim 1, AAPA discloses a latch either for sampling and latching continuous video data or for latching a latched result from an upstream sampling latch, said latch comprising: a CMOS latch cell (Fig.2 (7) [0008], [0009]); a power switch (fig.2 (12)) for connecting said CMOS latch cell to a power supply (Fig.2 VDD1, VDD2, VSS1, VSS2), [0008], [0011]; and an input switch disposed at an input of said CMOS latch cell (Fig.2 (7) [0008], [0009]); wherein said power switch and said input switch are switched on and off complementarily in such a manner that, with said CMOS latch cell disconnected from said power supply( [0008],[0011],(fig.2) VDD1,VDD2,VSS1,VSS2),, data to be latched is set on said CMOS latch cell and that, with said input of said CMOS latch cell ((Fig.2 (7) [0008],[0009]); disconnected from an upstream circuit, said power supply to said CMOS latch cell(Fig.2 (7) is switched on to level-shift ( [0011], [0016], fig.3F) the data set on said CMOS latch cell (fig.2 (7)). AAPA, however, does not disclose a digital-to-analog converter circuit. On the other hand, Nakajima discloses a digital-to-analog converter circuit (fig. 1, 125).

AAPA and Nakajima are analogous arts because they are from the same field of endeavor namely driving circuit.

At the time of the invention it would have been obvious to a person having ordinary skill in the art to add digital-to-analog converter circuit as taught by Nakajima to

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the driver circuit of AAPA to ensure a conversion of digital signal outputted from the line latch circuit to an analog signal.

The suggestion for doing would have been that the use of DAC is for converting a digital data into an analog data, which uses in a device that has analog signal input [0008].

Therefore it would have been obvious to combine AAPA with Nakajima for the benefit of a source driver circuit for an active matrix with a digital-to-analog converter circuit to obtain the invention.

As to claim 2, AAPA discloses a latch driving method for driving a latch comprising a CMOS latch cell either for sampling and latching continuous video data or for latching a latched result from an upstream sampling latch ([0007], [0008], [0009],), said latch driving method comprising the steps of: with said CMOS latch cell disconnected from a power supply ([0008], [0011] fig.2 VDD1, VDD2, VSS1, VSS2) connecting an input of said CMOS latch cell to an upstream circuit ((fig.2 (3))[0001]) so as to set corresponding data on said CMOS latch cell and with said input of said CMOS latch cell disconnected from said upstream circuit, switching on said power supply to said CMOS latch cell so as to level-shift the data set on said CMOS latch cell ((fig.2 (7) [0011], (fig.3F)).

As to claim 3, AAPA discloses A flat display apparatus comprising a display unit with pixels disposed in a matrix [0002], [0013] and driving circuits for driving pixels of said display unit [0020], said display unit and said driving circuits being formed integrally on a substrate [0002]; wherein said driving circuits include a horizontal driving

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circuit for setting gradations for said pixels of said display unit, said horizontal driving circuit including (fig.2 [0006]: a sampling latch [0007] for successively latching continuous video data (fig.2 (4) ,[0007]); a second latch for latching a latched result from said sampling latch on a line-by-line basis; and a digital-to-analog converter circuit for converting an output of said second latch from digital to analog form for output to said display unit [0020]; and wherein either said sampling latch or said second latch acts in such a manner that, with a CMOS latch cell is disconnected from a power supply [( [0008],[0011] fig.2 VDD1,VDD2,VSS1,VSS2)], an input of said CMOS latch cell is connected to an upstream circuit so as to set corresponding data on said CMOS latch cell and that, with said input of said CMOS latch cell disconnected from said upstream circuit ( (fig.2(3), [0001], said power supply to said CMOS latch cell is switched on to level-shift the data set( [0011], ( fig.3F ) on said CMOS latch cell (fig.2 (7)).

## Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Hailemariam whose telephone number is 571-270-1545. The examiner can normally be reached on M-F 8:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-270-1550. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Emmanuel Hailemariam

07/10/07

AMARE MENGISTU /